APPLICATION NOTE

AP-101

April 1981

The 2816 — Electrical Description

John F. Rizzo
Special Products Division
Applications Engineering

AFN-01913A

Flexibility, non-volatility, and a highly consistent system architecture — those attributes characterize the 2816 Electrically Erasable PROM. In this application note the electrical parameters that define the performance and operation of the device will be discussed. The concept of EPROM-like read architecture, encompassing high speed and 2-line control is detailed. In addition, the write/erase access needs some discussion as well. In the context of this discussion, the device performance, in its entirety, will be considered. In other application notes (Ap 102 and Ap 105), the system hardware and software architectural implications are discussed in detail.

INTRODUCTION

The 2816 is a 2K × 8 bit PROM that is electrically erasable. It's contents can be changed in the system without necessary removal from a board or cabinet. Along with this dramatic flexibility, the 2816 is non-volatile, just like the EPROM. The E^2 then benefits the user with EPROM-like data integrity and the additional capability to alter the memory data in-system. These two capabilities have never been possible with semiconductor memories. In addition to retaining data like the EPROM, the 2816 has very fast read access; data can be obtained from the device in less than 250 ns. This benefits system designers with high system performance to allow very competitive product entries.

The inherent flexibility that 2816 technology offers comes from the ability to alter single bytes of information. That is, just like a RAM, one byte of information can be erased and rewritten. Single-line editing of information is now possible. Direct register to memory transfer can occur without using additional and costly RAM buffer, which is unlike bulk erasable devices. In addition, if one wishes to erase the entire device at once, then a chip erase function is available. With this operation, all 2048 bytes of data can be returned to Logic 1 in 10 ms. The entire memory can be erased 300 thousand times faster than conventional EPROMs.

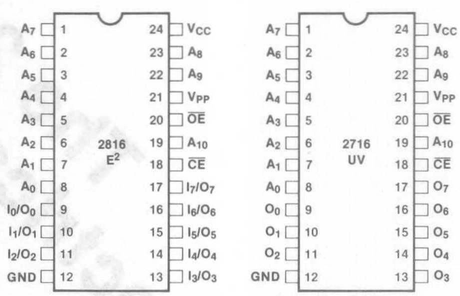
Because of the capability to write and erase data in-system, the 2816 architecture is designed to be very consistent. That is, the interface to the conventional microprocessor is simple and straight forward — unweildy and costly interface circuits are unnecessary. In the following paragraphs the read access, erase access, and write access modes will be discussed.

READ ACCESS MODE

The 2816 pinout, shown in Figure 1, is nearly identical to that of the 2716 EPROM. In the read mode, there are 3 groups of pins that are relevant: address, data, and control. The address input pins simply direct information within the device to be placed on the data output pins. When either of the control pins, $\overline{CE}$ or $\overline{OE}$ is logic "1", the data output pins are tri-stated. The combination of these control pins, called 2-line control, eliminates bus contention problems commonly encountered in microprocessor systems.

Chip enable is used as the primary device selection mechanism, and typically is obtained from address decoders. If chip enable alone is used to strobe data from the device to a common data base, then serious bus contention problems can result. Bus contention timing, shown in Figure 2, indicates why bus contention occurs. Basically, when one device on a common data bus is turned on, its outputs transition to either high or low levels. When it is deselected, there is a finite time delay before the output goes high impedance (this delay is a T_{DF} time which is specified in the data sheets).

Contention occurs, as shown, when one device is turning on while another is turning off. The timing overlap causes the data pins to be illegally driven from two sources. On any memory device with a single selection pin, system level bus contention can occur. Intel has pioneered the solution to bus contention through the use of the output enable pin. Output enable, as mentioned, simply strobes the output buffer. When output enable is connected to the microprocessor $\overline{RD}$ (read) line, contention is eliminated because no timing overlap can occur (as shown in Figure 3). Note that $\overline{CE}$ (derived from addresses) occurs far outside the $\overline{OE}$ signal — no overlap is thus possible. The two line control architecture of the 2816 therefore eliminates bus contention problems.



PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
V_{PP}	PROGRAM VOLTAGE

Figure 1. 2816 Pinout

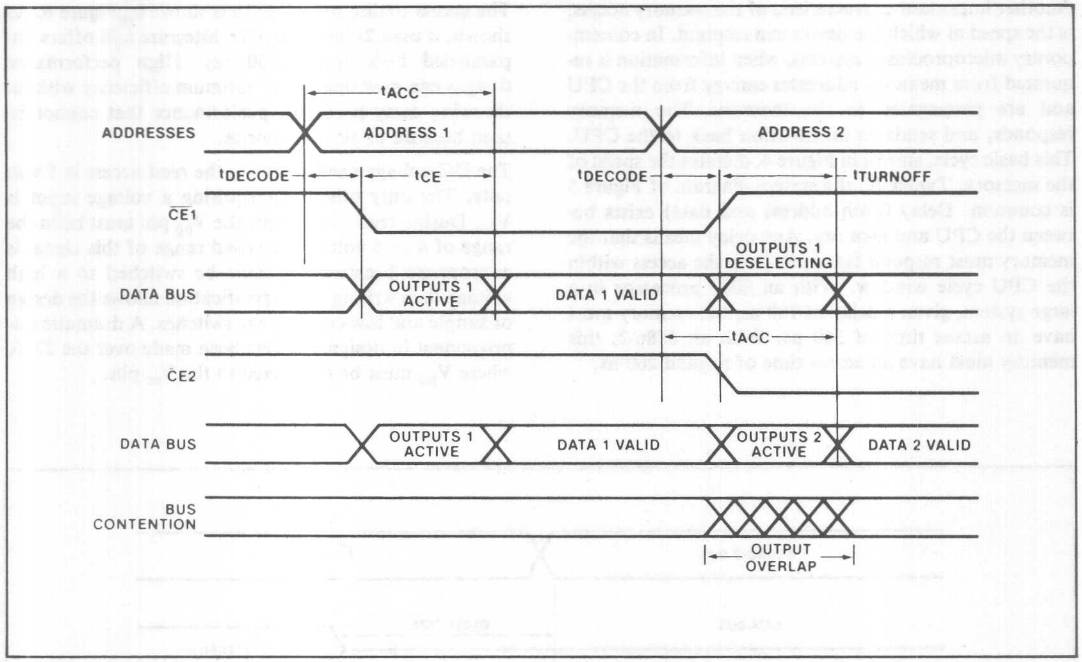


Figure 2. Single-Line Control and Bus Contention

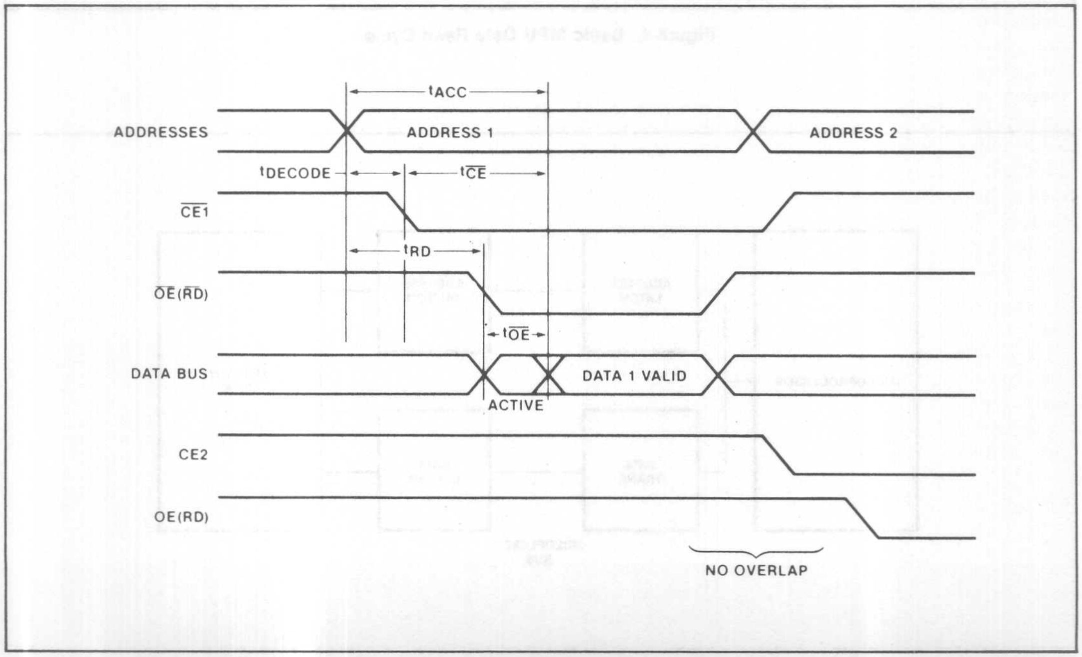


Figure 3. Two-Line Control Architecture

Another important characteristic of the memory access, is the speed at which the device can respond. In contemporary microprocessor systems, when information is requested from memory, addresses emerge from the CPU and are propagated to the memory. The memory responds, and sends its information back to the CPU. This basic cycle, shown in Figure 4, dictates the speed of the memory. Typically, the system diagram of Figure 5 is common. Delay (both address and data) exists between the CPU and memory. Any delay means that the memory must respond faster, to keep the access within the CPU cycle window. With an 8088 processor in a large system, given a delay of 100 ns, the memory must have an access time of 360 ns. With an 8086-2, this memory must have an access time of around 200 ns.

The access timing for the 2816 is shown in Figure 6. As shown, it used 2-line control architecture and offers unparalleled high speed (250 ns). High performance designs can now operate at optimum efficiency without throwing away processor performance that cannot be used because of slow memories.

The DC voltage needed during the read access is 5 volt only. The only other pin requiring a voltage input is V_{pp}. During read operations, the V_{pp} pin must be in the range of 4 to 6 volts. The broad range of this signal is appropriate because V_{pp} must be switched to a high voltage then writing. The specification allows the design of simple and low cost voltage switches. A dramatic improvement in design ease has been made over the 2716, where V_{pp} must be connected to the V_{cc} pin.

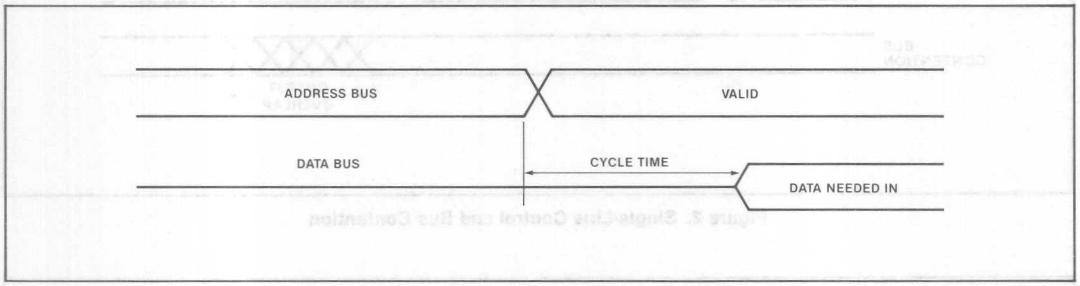


Figure 4. Basic MPU Data Read Cycle

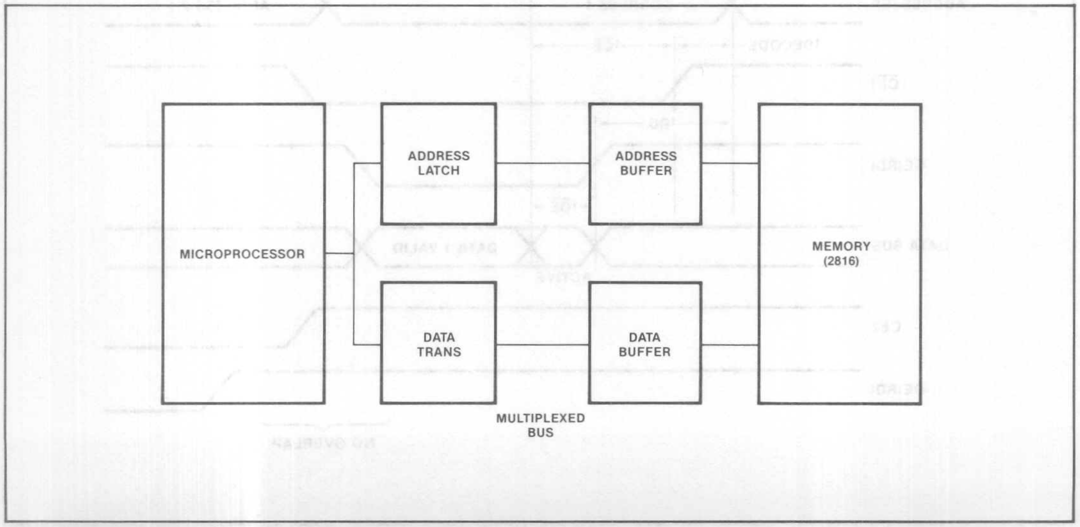


Figure 5. Common System Architecture

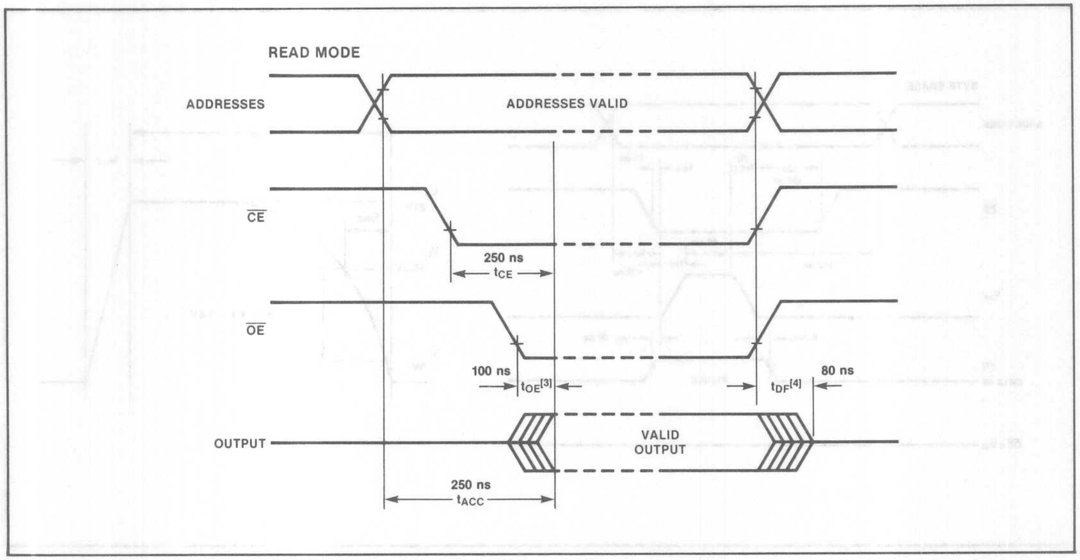


Figure 6. 2816 Read Access Timing

ERASE ACCESS MODE

The information stored in 2816 memory can be erased or changed through the application of simple electrical signals. A single, 10 ms, 21 volt pulse is all that is necessary to change any byte of information. The byte of data that needs to be altered must first be erased, then written.

The erase operation occurs automatically when certain information is presented to the 2816. In most cases, the byte must be erased prior to a data write. Whenever a bit within a byte must transition from a Logic 0 to 1, that byte must first be erased. Transitions from 1's to 0's can occur without an erase operation. Reasons behind the necessity for byte erase have been discussed in AR-118.

Mode selection for the 2816 is shown in Figure 7. The careful reader will note that the write and erase modes are basically identical with exception of the data input pins. When the input pins are all Logic Level "1", an automatic erase operation occurs. When a data pattern of ones and zeroes are presented, that data pattern is imbedded into the 2816 array. To accomplish byte erase the 2816 is selected by bringing $\overline{CE}$ to a logic Low. The address is provided to the device as well. To erase, a data input is set to "FF" Hex. The V_{pp} is then pulsed, through an exponential, to 21 volts. The timing diagram for this operation is shown in Figure 8. Note that there are set-up time requirements for address and V_{pp} to chip enable. At the completion of the write cycle, there are hold time requirements from V_{pp} as well. V_{pp} must rise through an exponential specified by an RC time constant, and be held for a minimum of 9 ms. V_{pp} can fall as quickly as possible, in fact, V_{pp} should be driven to 4 to 6 volts immediately to allow reading from the device, after a write. V_{pp} must rise slowly to 21 volts to allow low-level cell current flow to minimize cell voltage potentials. Simple circuitry is needed to provide this rise, and is explained in AP 102. During the entire erase cycle the output enable pin is kept at a VIH level. This makes much sense from a system compatibility standpoint since $\overline{OE}$ is an active low signal for read functions, and when high is inactive for erase/write functions.

In the erase mode $\overline{CE}$ is brought low. Microprocessor consistancy is preserved in this case as well because $\overline{CE}$ is derived from decoded addresses. The same address decoding circuitry — and nothing more — can be used to select the device in either READ or ERASE modes. This makes the system implementation very simple and straightforward.

MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	INPUTS/ OUTPUTS
READ	V_{IL}	V_{IL}	+4 to +6	D_{OUT}
STANDBY	V_{IH}	DON'T CARE	+4 to +6	HIGH Z
BYTE ERASE	V_{IL}	V_{IH}	+21	$D_{IN} = V_{IH}$
BYTE WRITE	V_{IL}	V_{IH}	+21	D_{IN}
CHIP ERASE	V_{IL}	+9 to +15V	+21	[11] $D_{IN} = V_{IH}$
E/W INHIBIT	V_{IH}	DON'T CARE	DON'T CARE	HIGH Z

Figure 7. Mode Selection $V_{CC} = \pm 5V$

AFN-01913A

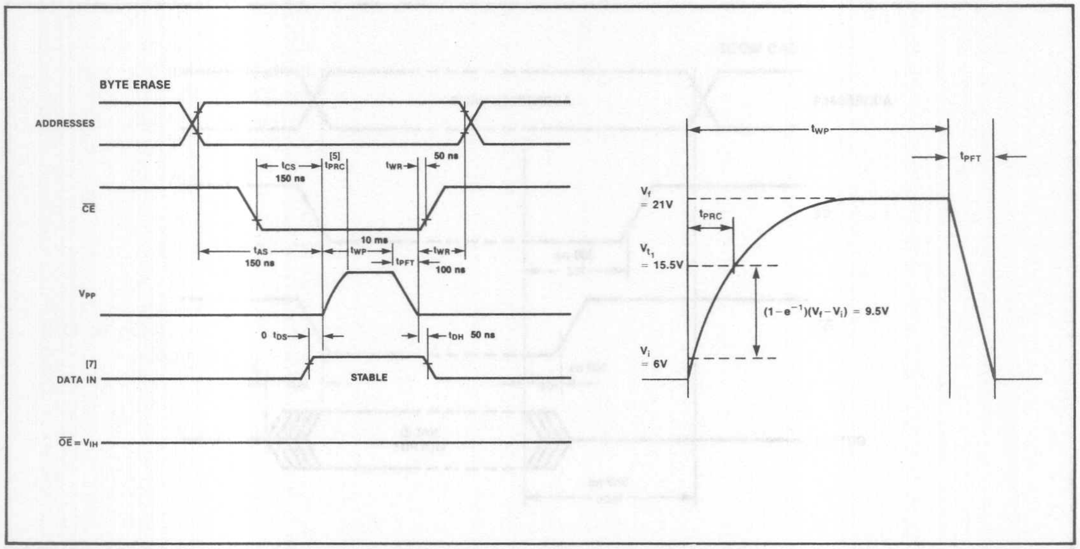


Figure 8. Byte Erase Timing

WRITE ACCESS

From the standpoint of functionality, the write access mode is identical to the erase mode. All setup times, hold times, voltage and timings are the same as used to erase the device. The only difference in operation is the data that is presented to the 2816. When a write is to occur, the data that is to be written is simply supplied to the device. The V_{PP} pin is pulsed exactly as before, all rise times and timings are consistent with the erase mode.

The timing diagrams for the write mode are shown in Figure 9. Also noted in that Figure are the actual device timing parameters.

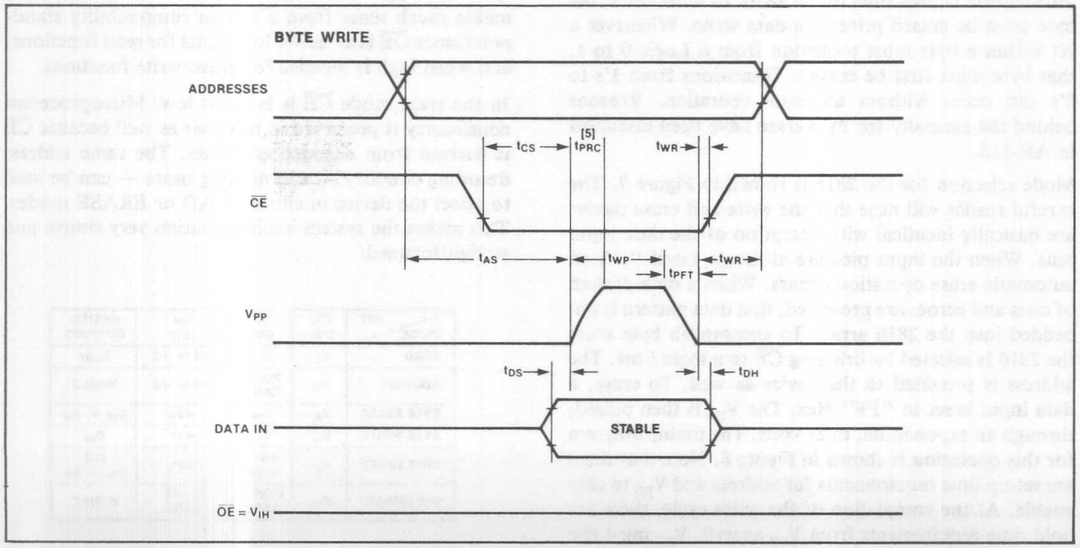


Figure 9. Byte Write Timing

In general, the 2816 has been designed to allow simple and straight forward mode selection and timing. In the erase/write mode, the control and functional pin designations reflect an in-system writable architecture. The design closely approximates RAM architecture to make system design easy.

The 2816 differs substantially from the 2716 EPROM in the write mode. The mode select tables for both devices are shown in Figure 10. In all cases, the 2816's functionality optimizes read and write operations above and beyond those inherent in the 2716 EPROM. All of the modes reflect a goal of simple designs in microprocessor systems.

IMPROVED IMPROVED

MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	INPUTS/ OUTPUTS	
READ	V_{IL}	V_{IL}	+4 to +6	+5	D_{OUT}	2816
	V_{IL}	V_{IL}	+5	+5	D_{OUT}	2716
STANDBY	V_{IH}	DON'T CARE	+4 to +6	+5	HIGH Z	2816
	V_{IH}	DON'T CARE	+5	+5	HIGH Z	2716
BYTE ERASE	V_{IL}	V_{IH}	+21	+5	$D_{IN} = V_{IH}$	2816
	N/A	N/A	N/A	N/A	N/A	2716
BYTE WRITE (PROGRAM)	V_{IL}	V_{IH}	+21	+5	$D_{IN} = D_{IN}$	2816
	V_{IH}	V_{IL}	+25	+5	$D_{IN} = D_{IN}$	2716
E/W (PROGRAM) INHIBIT	V_{IH}	DON'T CARE	DON'T CARE	+5	HIGH Z	2816
	V_{IL}	V_{IH}	DON'T CARE	+5	HIGH Z	2716

IMPROVED IMPROVED IMPROVED

Figure 10. 2716 Mode Selection

CHIP ERASE ACCESS

In order to erase all 2K bytes in 10 ms, special signalling is required. The output enable pin has been multiplexed for Chip Erase functions. To put the 2816 in that mode, $\overline{OE}$ is set in the range of 9 to 15 volts. Once engaged, the chip erase occurs by simply pulsing V_{pp} and $\overline{OE}$ in the same way as the write and erase modes. While a higher voltage is needed to perform chip erase, virtually no current flows into the $\overline{OE}$ pin. A standard 10 μA leakage current is specified over the full voltage range.

The timing diagrams and specifications for this mode are shown in Figure 11. The careful reader will notice that all of the signals (with the exception of $\overline{OE}$) are identical to the write/erase access modes.

DC VOLTAGE CONDITIONS

In the write and erase modes, the V_{PP} signal must be held within the 20 to 22 volts operating range. The 21 volt typical voltage is derived from Intel's patented HMOS-E processing. In the long term this will become a standard level for program voltages. If greater than the maximum of 22 volts is applied to the 2816, permanent and destructive device damage will result. If less than 20 volts is applied, then long term data retention is not guaranteed. The DC specification for the device is shown in Figure 12.

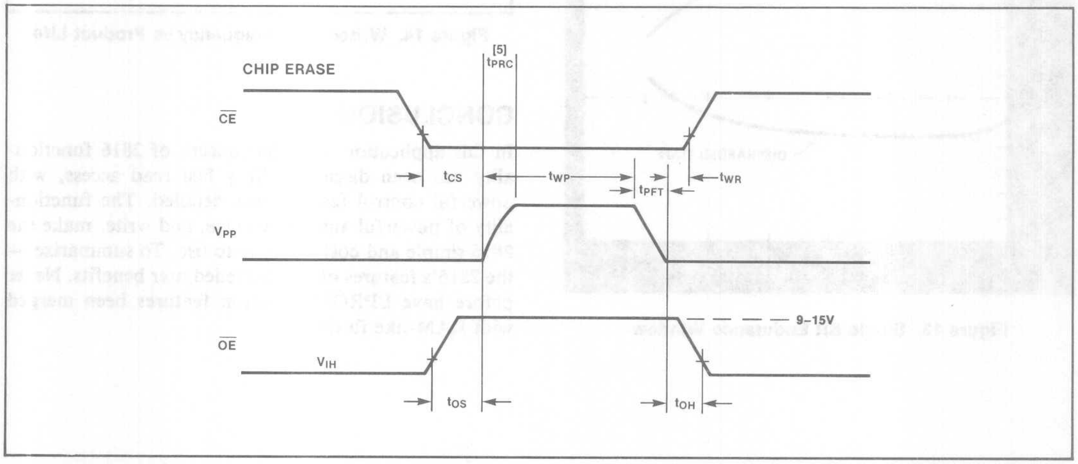


Figure 11. Chip Erase Timing

AFN-01913A

WRITE OPERATION

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{PP}	WRITE/ERASE VOLTAGE	20	21	22	V	
$I_{PP(W)}$	V_{PP} CURRENT (WRITE/ERASE)			15	mA	$\overline{CE} = V_{IL}$
V_{OE}	$\overline{OE}$ VOLTAGE (CHIP ERASE)	9		15	V	$I_{\overline{OE}} = 10\mu A$
$I_{PP(I)}$	V_{PP} CURRENT INHIBIT			5	mA	$V_{PP} = 21$, $\overline{CE} = VIH$

Figure 12. Write/Erase DC Parameters

ENDURANCE ISSUES

The 2816 has a characteristic ceiling on the number of erase/write cycles that can be endured. This ceiling exists because the cell threshold window changes (or closes) as the device is cycled.

Eventually, the device becomes permanently erased. Figure 13 shows how the single bit window changes.

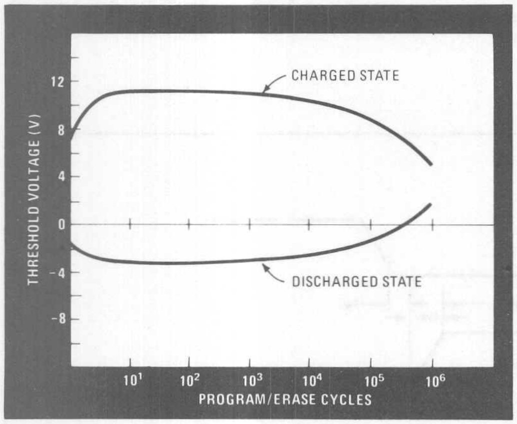


Figure 13. Single Bit Endurance Window

The E^2PROM from Intel is specified to handle 20,480,000 erase/write cycles per chip. Each byte can be cycled up to 10,000 times, and each byte operates independently of any other. Given a ten year machine life, each byte can be cycled up to 3 times per day. Figure 14 shows a graph relating product life and maximum write/erase frequency. In the majority of applications, less than 3,000 cycles are required.

This makes the 2816 an ideal device for those systems.

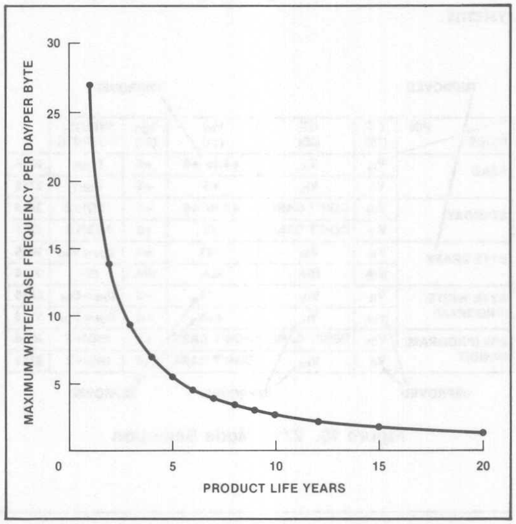


Figure 14. Write/Erase Frequency vs Product Life

CONCLUSION

In this application note the concept of 2816 functionality has been discussed. Very fast read access, with powerful control features was detailed. The functionality of powerful automatic erase, and write, make the 2816 simple and cost-effective to use. To summarize — the 2816's features offer unexcelled user benefits. Never before have EPROM retention features been merged with RAM-like flexibility.